The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte ROBERT VARNEY

MAILED
MAR 17 2006
U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Appeal No. 2006-0839
Application No. 10/003,982

ON BRIEF

Before KRASS, RUGGIERO and BARRY, Administrative Patent Judges.
KRASS, Administrative Patent Judge

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 24-27, 32-35, and 37-44.

The invention pertains to testing devices and a display of the test results. In particular, a design-for-test (DFT) is applied to look for manufacturing defects, such as in semiconductor devices. A series of interconnected flip-flop cells is included in chip designs in order to take advantage of such DFT testing. These series of cells are known as "scan chains"; the testing of these scan chains involving serially shifting data through the cells and determining whether the correct outputs show up at the last scan cell. Scan chain failure information has been tabulated in a list format, noting the identification of the

scan chain and its relative location in the chip. When hundreds of devices are tested simultaneously, the list of such scan chain failure information can become unwieldy and not readily comprehensible.

The instant invention seeks to improve the presentability of the data into a format that is readily comprehensible to a test engineer, by using a graphical user interface (GUI) generator to condense failed scan chain data into a file that is then used to generate graphical representations of the scan chains. The lower rectangular area of instant Figure 8 is representative of the graphical representation.

Representative independent claim 24 is reproduced as follows:

24. A DFT result diagnosis system including:

an ATE data source for providing test data in the ATE domain;

an ATPG tool operative to generate ATPG pattern data and ATPG results data in the ATPG domain;

at least one translation module to automatically convert data between multiple domains;

at least one function module to automatically summarize data from one or more devices or tests in one or more domains;

a graphical user interface generator for receiving data identifying failed scan chains and scan cells from the ATE data source and ATPG tool and generating graphical representations of the failed scan chains and cells; and

a display device coupled to receive the graphical representations from the graphical user interface, the display device operative to display the graphical representations of the failed scan chains.

The examiner relies on the following references:

Smith et al. (Smith)	6,185,707	Feb. 06, 2001
Testa et al. (Testa)	6,205,407	Mar. 20, 2001

Claims 24-27, 32-35, and 37-44 stand rejected under 35 U.S.C. §103 as unpatentable over Smith in view of Testa.

Reference is made to the brief and answer for the respective positions of appellant and the examiner.

OPINION

Appellant separates the claims into two groups for appeal purposes. Group I consists of claims 24-27 and 32-35. Group II consists of claims 37-44. Accordingly, we will concentrate on independent claim 24 as being representative of the claims in Group I and on independent claim 37 as being representative of the claims in Group II.

In rejecting claims under 35 U.S.C. §103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teachings, suggestions or implications in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc. , 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d

1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the *prima facie* case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See Id.; In re Hedges, 783 F.2d 1038, 1040, 228 USPQ 685, 687 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1051, 189 USPQ 143, 146-147 (CCPA 1976). Only those arguments actually made by appellant have been considered in this decision. Arguments which appellant could have made but chose not to make in the brief have not been considered and are deemed to be waived [see 37 CFR §41.67(c)(1)(vii)].

With regard to claim 24, the examiner applies the references as follows:

The examiner points to Figures 11 and 12, and column 3, lines 1-12, of Smith for a teaching of a DFT result diagnosis method and system including an ATE data source, an ATPG tool to generate ATPG pattern data, at least one translation module, and means to summarize test result data. In fact, the examiner indicates that the only element of the claim not disclosed by Smith is the GUI for displaying results.

The examiner then turns to Testa for a teaching of generating test code for testing an IC on an ATE platform that includes translating scan and pattern data into test code that makes use of a GUI, pointing to the Abstract, Summary of Invention, and column 2, lines 25-56, of Testa.

The examiner concludes that it would have been obvious to combine the teachings of Smith and Testa to obtain the claimed subject matter since "GUI's and other graphics would greatly facilitate and enhance the scan diagnosis process, and are now well known in the art of IC design and development" (Final rejection, Mar. 22, 2004 - page 4).

Appellant argues that there is no motivation to use the list of failed scan chains by itself, much less take on the additional effort to display a graphical representation of the failed scan chains. Appellant also argues that Testa has no relevance to the field of design-for-test (DFT) automatic test equipment (ATE) or to failure diagnostics, teaching, instead, pattern generation, the opposite of diagnosis.

In particular, appellant argues that the Group I claims distinguish over the Smith/Testa combination by the recitation of a graphical user interface generator for generating graphical representations of failed scan chains.

We have reviewed the evidence before us, including the disclosures of Smith and Testa, as well as the arguments of appellant and the examiner, and we conclude therefrom that the examiner has not established a *prima facie* case of obviousness with regard to the subject matter of claim 24.

While Smith is clearly directed to DFT result diagnosis systems, as claimed, Smith appears to take the output of a functional tester and then translate it from a list of failed scan chains into a list of suspected netlist nodes (see Abstract and column 3, lines 1-11). That is, unlike the instant claimed subject matter, Smith does not use a GUI generator for receiving data identifying those failed scan chains and then generating graphical representations of the failed scan chains. While Testa does disclose a GUI, e.g., Abstract, the GUI of Testa is used by a user to define certain custom format features for output test data. There is no suggestion in Testa that the system disclosed therein would have any applicability to DFT automatic test equipment, nor is there any indication that the GUI in Testa receives data identifying failed scan chains and then generates graphical representations of the failed scan chains, as claimed.

Accordingly, there would appear to be no reason for the skilled artisan having these two references before him/her to have made the combination proposed by the examiner. Since neither one of Smith or Testa suggests the claimed feature of using a GUI generator for receiving data identifying failed scan chains and then generating graphical representations of the failed scan chains, and we find no reason for making the combination in any case, we will not sustain the examiner's rejection of claims 24-27 and 32-35 under 35 U.S.C. §103.

With regard to claim 37, this claim requires a sequence of instructions wherein scan failure data is captured, a portion of the scan chains including the captured failure data is graphically displayed and a diagnosis is made of the scan failure data.

The examiner employs the same reasoning as above, adding that Smith teaches how the X-Y coordinates of a failed net (i.e., a failed scan chain) can be identified and displayed, so that they can be easily diagnosed.

Appellant distinguishes the instant claimed subject matter from the applied references in pointing to the claimed "graphically displaying a portion of the scan chains including the captured failure data." Appellant also points out that the examiner's equating a failed net with a failed scan chain is in error because Smith goes to great lengths to explain the difference between scan chains, representing regions of logic, and netlist nodes, which are transistor-level connections (see page 9 of the brief). Thus, while appellant admits that Smith teaches how to identify and display X-Y physical coordinates of a failed netlist node, this is "fundamentally different than graphically displaying scan chains" (brief-page 9).

The examiner's response is that Smith teaches the failed netlist nodes as another representation of the failed scan chains (answer-page 7). The examiner bases this

reasoning on Smith's disclosure of taking the failed scan chain out (column 3, lines 46-53) and translating it into a list of suspected (i.e., failed) netlist nodes which can be displayed graphically (Smith-Figure 7, or Testa's GUI as described in the Abstract).

Even assuming what the examiner alleges to be true, by the examiner's own admission, Smith takes the failed scan chains and translates them into netlist nodes. By translating such data, Smith is no longer using failed scan chains when and if such data is displayed. Moreover, the examiner has not sufficiently rebutted appellant's point about Smith's distinguishing between the two concepts by defining scan chains as a discrete chain of logic which can be tested individually (Smith, column 2, lines 51-53) and netlist nodes as a list of low level design cells and the interconnections between them (Smith, column 1, lines 22-24).

Since Smith does distinguish between netlist nodes and scan chains, the examiner's attempt to equate them, within the disclosure of Smith, appears at odds with the very disclosure of Smith. Since Smith does not describe displaying a portion of the scan chains including the captured failure data, as claimed, and Testa is no help in this regard, we will not sustain the examiner's rejection of claims 37-44 under 35 U.S.C. §103.

The examiner's decision rejecting claims 24-27, 32-35, and 37-44 under 35 U.S.C. §103 is reversed.

REVERSED

ERROL A. KRASS
Administrative Patent Judge

JOSEPH F. RUGGIERO
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

) BOARD OF PATENT APPEALS AND INTERFERENCES

EK/gw

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